1 INTRODUCTION

Manson et al. [2005] identify the central problem in the design of software relaxed memory models: “The memory model must strike a balance between ease-of-use for programmers and implementation flexibility for system designers.”

There are two aspects to “ease of use.” First, programs should support compositional and local reasoning; in this paper, we emphasize temporal safety properties [Abadi and Lamport 1993; Misra and Chandy 1981; Pnueli 1984; Stark 1985]. Second, relaxed memory should be not change the behavior of correctly synchronized programs; this property is known as sequential consistency for data race free programs (sc-drf) [Adve and Hill 1990, 1993].

There are also two aspects of “implementation flexibility.” First, relaxed atomic access should not require hardware synchronization (at least for the word size of the machine). Second, the model should facilitate compiler transformations, such as the reordering of independent statements; ideally the model should support all optimizations of synchronization-free single-threaded code.

Sailing between this Scylla and Charybdis has proven very difficult. Three lines of code can leave the top experts in the field flabbergasted. The solutions that have been proposed are understandable to mechanical proof assistants, but humans have been left behind.
In this paper, we combine two ideas that humans can understand: preconditions [Hoare 1969] and labelled partial orders (aka pomsets) [Gischer 1988; Plotkin and Pratt 1996]. The resulting model mostly satisfies the desiderata. We sacrifice only implementability on "non-mca" processors, such as POWER and ARM7. As a result, however, there is only one order relation to visualize.

Perhaps you believe the problem has already been solved? Let us try to convince you otherwise.

To get a sense of the difficulties involved, consider that the existence of an execution in a relaxed memory model may depend on code that was not executed. Let $r$ and $s$ be registers and $x$-$z$ be shared memory locations. Consider the following program, where all memory locations are initialized to 0:

$$y := x \parallel r := y; \text{if}(r)\{x := r; z := r\} \text{else} \{x := 1\}$$  

Most programmers would be surprised to learn that this program does allow an execution in which $z = 1$. To see why, imagine that a compiler does type inference and finds that $x$ and $y$ are booleans, with value either 0 or 1. This enables the program to be optimized to the following:

$$y := x \parallel r := y; \text{if}(r)\{x := 1; z := 1\} \text{else} \{x := 1\}$$  

Since $x := 1$ occurs in both branches of the conditional, the compiler can then lift it, and reorder with the independent read of $y$, yielding:

$$y := x \parallel x := 1; r := y; \text{if}(r)\{z := 1\}$$  

Then $z = 1$ at then end of an execution where the first thread is interleaved immediately after executing $x := 1$. Compare (*) with:

$$y := x \parallel r := y; \text{if}(r)\{x := r; z := r\} \text{else} \{x := 2\}$$  

which has a similar execution where $z = 2$, but does not have an execution where $z = 1$. Note that the only difference between (*) and (†) is the code in the branch that was not taken. This means that any model of relaxed memory that supports common compiler optimizations (such as the transformations above) must take into account code that was not executed. This is why most relaxed memory models include some form of speculative execution.

Pugh [1999, §2.3] initiated the modern study of relaxed memory by noting that Java 1.1 failed to validate Common Subexpression Elimination (CSE) in the presence of aliasing. For example, given that $r_2 \neq s$, is it valid to transform the program on the left to that on the right?

$$(r_1 := x; s := y; r_2 := x; C) \quad (r_1 := x; r_2 := r_1; s := y; C)$$

The resulting Java Memory Model (JMM) [Manson et al. 2005] greatly advanced the state of the art. Lochbihler’s monumental study of the JMM revealed a surprising limitation. Consider the following program [Lochbihler 2013, Fig. 8], where again all memory locations are initialized to 0:

$$y := x \parallel r := y; \text{if}(z)\{r := \text{new}D\} \text{else} \{s := \text{new}C\}; x := r \parallel z := 1$$  \hspace{1cm} \text{ooota1}$$

is type correct if it declares $x$, $y$ and $r$ of type $D$. However, it has a legal execution where they reference a $C$ object. The JMM allows $(r := y)$ to see the object created by new, by bouncing it through $(x := r)$ and $(y := x)$. This allows the address of the allocated object to be read $(r := y)$ before its type is determined (if $(z)$). For a simpler variant without allocation, see ooota4 in §6.

By allowing such bait-and-switch behaviors, the JMM fails to support compositional reasoning for temporal safety properties: the individual threads of ooota1 satisfy the invariant allocation at type $C$ is preceded by reading 0 for $z$, but the composed program does not. This lack of compositionalty forced Lochbihler to partition memory by type in order to prove type safety. This formal device means that memory cannot be used at different types over time, making practical memory reclamation impossible. Even with this solution for type safety, there are implications for the Java security architecture [Lochbihler 2013, §5.4].
As confirmed by [Chakraborty and Vafeiadis 2018; Kang et al. 2018], the promising semantics [Kang et al. 2017] and related models [Chakraborty and Vafeiadis 2019; Jagadeesan et al. 2010] all allow oota4, invalidating compositional reasoning for temporal safety properties. This means that these models cannot support both type safety and realistic memory reclamation.

The C11 Memory Model [Batty et al. 2011] does not attempt to validate CSE, at least not for relaxed atomic access (consider the case where \(x\) and \(y\) are aliased above). C11 does allow the transformation for plain access, but this comes with the threat of undefined behavior should any plain access ever possibly engage in a data race [Boehm 2007]. C11 also allows values that arise “Out Of Thin Air” (oota) [Batty et al. 2015], exploiting causality cycles. Undefined and oota behaviors are antithetical to the goals of safe languages.

Strong models, including Sequential Consistency (SC) [Lamport 1979], RC11 [Lahav et al. 2017], and others [Boehm and Demsky 2014; Dolan et al. 2018; Jeffrey and Riely 2016; Lahav et al. 2017] support compositional reasoning. However, all of these models invalidate reordering of independent statements. Several require fences after relaxed reads, even on ARM8.

**Our Model.** In our approach, a program is a set of executions. Each execution is a partial order on a set of read and write events. The order is intended to be read as a “dependency” relation. The dependency relation can vary between executions, so it is dynamic; events that are not related in an execution are “independent” and can be seen by a sequential observer in either order.

Cross thread dependencies arise from conflicting actions on the same variable: Roughly, we order any two actions on the same location, at least one of which is a write. In the parlance of hardware memory models [Alglave et al. 2014]: coe, fre, and rfe are included in the global dependency ordering. Thus, our model realizes multi-copy atomicity (mca): when a write becomes visible to one thread it must become visible to all [Pulte et al. 2018]. As envisioned in [Alglave 2010, §3.3], this allows us to capture cross-thread dependencies in a single partial order.

Our key insight is that mca permits a single, global notion of time, manifest in the pomset order. Within a thread, the dependency calculation can be viewed as the computation of preserved program order (ppo) in hardware models. ppo captures the essential dependencies between events in the same thread. Consider the following program fragments:

\[
C_1 : x := 1; y := 1 \\
C_2 : r := x; \text{if}(r) \{ y := 1 \} \text{else} \{ y := 1 \} \\
C_3 : x := 1; r := x; \text{if}(r) \{ y := 1 \}
\]

All these fragments satisfy \{true\} \(C_1 \{ y = 1 \}\); thus, in each case, the write of \(y\) is independent of any code that precedes it in program order. While \(C_1\) reflects syntactic independence, \(C_2\) reflects the independence derived by case analysis, and \(C_3\) reflects the independence deduced from partial evaluation (in the restricted form of constant propagation).

Our key insight is that logic is better than syntax to capture such dependencies.

The logical perspective provides a clear intuition as to why certain compiler transformations should be valid. Such intuitions are not always readily available in relaxed memory models. For example, value range analysis—used in the discussion of (*)—is very difficult in many models. As another example, models such as ARM8 distinguish internal reads, which are fulfilled by a write of the same thread, from external ones. Unlike externally fulfilled reads, internal reads are not necessarily recorded in the dependency relation. As exemplified by \(C_3\), this allows a compiler to reorder the fulfilling write with subsequent code that depends on the read. Neither value range analysis nor internal reads require special treatment in our model.

The executions of a program are computed compositionally, by induction on the structure of the program. Thus, our model falls into the style of relaxed memory models advocated by Batty [2017]. Combined with a single global order on events, compositionality helps explain how our
model disallows OOTA execution. After all, compositionality states that parallel composition does not create unexpected behaviors. The simplest OOTA litmus test is the following variant of (**) and OOTA1—without z or the conditional. Again all memory locations are initialized to 0:

\[
y := x \parallel r := y; x := r
\]

(OOTA2)

We rule out non-zero reads as follows: The write of \( y \) on the left hand side is dependent on the read to \( x \). Similarly, the write of \( x \) on the right is dependent on the read to \( y \). Since a non-zero read can only be satisfied externally, both reads are part of the dependency order, leading to a cycle. Such a cycle contradicts the assumption that dependency forms a partial order. We discuss OOTA1 in §6.

In §2 and §4, we define the model. We show that the model:

- validates expected litmus cases and compiler optimizations (§3-4).
- captures all C11 concurrency features (§5),
- allows compositional reasoning for safety, disallowing OOTA behavior (§6),
- is implementable on ARM8/TSO without extra synchronization for relaxed access (§7), and
- satisfies the local sc-DRF criterion [Dolan et al. 2018] (§8).

We conclude by discussing relating work (§9) and limitations (§10).

2 THE BASIC MODEL

The model adapts our previous work on microarchitecture [Disselkoen et al. 2019] to the architectural level. In this section, we define the model and use it to give the semantics of a concurrent language. The semantics given here is simplified: as discussed in §4, it fails to validate some important optimizations. We give the full semantics in §4. In §5, we define extensions that incorporate fences, read-modify-write operations, and address computation.

The model is based on partially ordered multisets [Gischer 1988; Plotkin and Pratt 1996], where events are labelled with reads and writes, and the partial order tracks dependencies, which arise within threads due to local dependencies and across threads due to reads and coherence.

For example the semantics of (**) contains the expected pomset (where \( \checkmark \) indicates termination):

\[
y := 0; x := 0; (y := x \parallel r := y; if(r){x := r; z := r} else {x := 1})
\]

\[
\begin{align*}
W_y0 & \quad W_x0 \\
R_x0 & \quad W_y0 \\
R_y0 & \quad W_x1 \\
\checkmark &
\end{align*}
\]

(*)

but also the unexpected one:

\[
\begin{align*}
W_y0 & \quad W_x0 \\
R_x1 & \quad W_y1 \\
R_y1 & \quad W_x1 \\
W_z1 & \quad \checkmark
\end{align*}
\]

(**)

The interesting fact about these pomsets is that there is no control dependency between reading \( y \) and writing \( x \), since the \( (W_x1) \) event happens on both sides of the conditional.

An attempt to replicate this execution with (†) fails, since it introduces a cycle:

\[
y := 0; x := 0; (y := x \parallel r := y; if(r){x := r; z := r} else {x := 2})
\]

\[
\begin{align*}
W_y0 & \quad W_x0 \\
R_x1 & \quad W_y1 \\
R_y1 & \quad W_x1 \\
W_z1 & \quad \checkmark
\end{align*}
\]

(†)

In this case, \( (W_x1) \) only happens on one side of the conditional, causing a control dependency from \( (R_y1) \) to \( (W_x1) \). In these diagrams, color plays no formal role. There is only one order. We use color only to help the reader see where the order comes from:

- \( (R_y1) \rightarrow (W_x1) \) is a local requirement, relating reads to writes that depend on them.
- \( (W_x1) \rightarrow (R_x1) \) is a reads-from requirement, relating writes to reads they fulfill.
- \( (W_x0) \rightarrow (W_x1) \) is a coherence requirement, relating actions that touch the same location.
- \( (W^{\circ2} z1) \rightarrow (\checkmark) \) is a fencing requirement, involving fences and synchronization actions.
In addition to actions, each pomset event is labeled with a **precondition**. Whereas read actions represent an obligation that must be **fulfilled** concurrently by a matching write (Def. 2.7), preconditions represent an obligation that must be **satisfied** sequentially via substitution.

To get a sense of how preconditions are satisfied, let us consider the evolution of the precondition of \((Wx1)\) during the calculation of \((\ast\ast)\). First consider the else-branch of the conditional: the semantics of \(\text{"if } \neg r \{ x := 1 \} \text{"} \) contains \((r=0) | Wx1\), indicating the control dependency. The then-branch is more complex: the semantics of \(\text{"if } r \{ x := r \} \text{"} \) contains \((r \neq 0 \land r = 1) | Wx1\) indicating both a control and a data dependency. This can be simplified to \((r=1) | Wx1\). Combining the two branches of the conditional, we have \((r=0 \lor r=1) | Wx1\). Prepending \(r := y\) substitutes \(\{ y/r \}\), resulting in \((y=0 \lor y=1) | Wx1\). Prepending the initializer \(y := 0\) substitutes \(\{ 0/y \}\), resulting in \((0=0 \lor 0=1) | Wx1\). This is a tautology, which we write as \((Wx1)\). We repeat this calculation in \(\S2.6\), after giving the formal definitions.

The same calculation fails for the write to \(x\) in \((\dagger)\). In this case, the writes to \(x\) on either side of the conditional cannot be combined, since one side writes 1 and the other side writes 2. Thus, the semantics of the conditional contains \((r=1) | Wx1\), rather than \((r=0 \lor r=1) | Wx1\). As we shall see, it is only possible to weaken this precondition by introducing order from \((Ry1)\) to \((Wx1)\).

### 2.1 Data models

A **data model** consists of:

- a set of **values** \(\mathcal{V}\), ranged over by \(v\) and \(\ell\),
- a set of **registers** \(\mathcal{R}\), ranged over by \(r\) and \(s\),
- a set of **expressions** \(\mathcal{M}\), ranged over by \(M, N\), and \(L\),
- a set of **memory locations** \(\mathcal{X}\), ranged over by \(x\) and \(y\),
- a set of **actions** \(\mathcal{A}\), ranged over by \(a\) and \(b\), and
- a set of **logical formulae** \(\Phi\), ranged over by \(\phi\) and \(\psi\).

Let \(\sigma\) range over substitutions of the form \([x/r]\) or \([N/x]\).

We require that data models satisfy the following:

- values, registers, and memory locations are disjoint,
- values include at least the constants 0 and 1,
- expressions include at least registers and values,
- expressions do not include memory locations,
- formulae include at least equalities \((M = v)\),
- formulae are closed under negation, conjunction, disjunction, and substitution,\(^1\)
- there is a relation \(\vDash\) between formulae, with the expected semantics.

For the actions of a data model, we require that there are partial functions \(\text{Rd} : \mathcal{A} \rightarrow (\mathcal{X} \times \mathcal{V})\), and there are subsets of \(\mathcal{A}\): Acq, Rel, SC, and Term, such that \(\text{dom}(\text{Rd}) \cap \text{SC} \subseteq \text{Acq}, \text{dom}(\text{Wr}) \cap \text{SC} \subseteq \text{Rel}, \text{and Term} \subseteq \text{Rel}\).

- We say that action \(a\) is a **read** if \(a \in \text{dom}(\text{Rd})\). We say that \(a\) is a **write** if \(a \in \text{dom}(\text{Wr})\). When \(\text{Rd}(a) = (x, v)\), we say that \(a\) **reads** \(v\) from \(x\), and similarly for writes. We say that \(a\) **accesses** \(x\) if it reads or writes \(x\).
- Actions in Acq, Rel and SC, are **synchronization** and **fencing** actions. We say that \(a\) is an **acquire** if \(a \in \text{Acq}\), \(a\) is a **release** if \(a \in \text{Rel}\), and \(a\) is **SC** if \(a \in \text{SC}\). We require that every SC read is an acquire, and every SC write is a release.
- Actions in Term are **termination** actions. We require that termination events are releasing.

---

\(^1\)Since formulae are closed under substitutions of the form \(\phi[x/r]\), they must include equalities of the form \((M = v)\) where \(M\) is an **extended expression** that includes memory locations. By composition, formulae must also be closed under that substitutions of the form \(\phi[M/r] = \phi[x/r][M/x]\).
Our example language includes actions of the form $(\theta)$, which is a termination, $(R^\mu x v)$, which reads $v$ from $x$ and $(W^\mu x v)$, which writes $v$ to $x$. The access mode $(\mu ::= rlx \mid ra \mid sc)$ is either relaxed, release-acquire, or sequentially-consistent. ra/sc reads are acquires, and ra/sc writes are releases. We systematically elide the rlx-mode annotation, writing $(R x v)$ as shorthand for $(R^\mu x v)$.

We do not explicitly include C11-style plain access. If thin-air executions are disallowed, plain access is the same as relaxed access for data race free programs; data races on plain access result in undefined behavior [Boehm 2007].

Logical formulae include equations over locations and registers, such $(x=1)$ and $(r=s+1)$. We use expressions as formulae, coercing $M$ to $M \neq 0$.

Formulae are open, in that occurrences of register names and memory locations are subject to substitutions of the form $\phi[x/r]$ and $\phi[N/x]$. Actions are not subject to substitution.

**Definition 2.1.** We say $\phi$ is independent of $x$ if, for every $v$, $\phi \Rightarrow \phi[v/x] \equiv \phi$; it is dependent otherwise. We say $\phi$ is location independent if it is independent of every location. We say $\phi$ implies $\psi$ if $\phi \Rightarrow \psi$. We say $\phi$ is a tautology if $true \Rightarrow \phi$. We say $\phi$ is unsatisfiable if $\phi \Rightarrow false$.

### 2.2 Semantic domain

We model single executions as pomsets with preconditions—pomsets, for short—ranged over by $P$. These extend the well-known model of partially ordered multisets [Gischer 1988] with formulae.

The pomset order relation, $\leq$, represents causality or dependency. We visualize pomsets as directed graphs. For example, the semantics of $\texttt{var } x; (x:=0); x:=1 \parallel y:=x; z^{ra}:=1$ includes:

![Diagram of pomsets]

We visualize order using arrows that indicate the reason that the order arises. $(W x 0) \rightarrow (W x 1)$ is a coherence requirement: the write of $1$ must follow the write of $0$, since these are in conflict and in program order. $(W x 1) \rightarrow (R x 1)$ is a reads-from requirement: the read of $x$ must be fulfilled by a matching write. $(R x 1) \rightarrow (W y 1)$ is a local dependency requirement: the write to $y$ is data dependent on the read of $x$; control and address dependencies are also local. $(W y 1) \rightarrow (W^{ra} z 1)$ and $(W^{ra} z 1) \rightarrow (\theta)$ are fencing/synchronization requirements.

Since each pomset represents a single execution, we require that all preconditions be consistent. For example, the semantics of if $(r < 0) \{y:=1\} \text{ else } \{z:=1\}$ includes pomsets with either $(r < 0 \mid W y 1)$ or $(r \geq 0 \mid W z 1)$, but not with both, since $(r < 0 \land r \geq 0)$ is unsatisfiable.

Preconditions are linked to pomset order via causal strengthening, which requires that formulae do not weaken over time, as measured by $\leq$. Example oota3 (§5) requires causal strengthening.

**Definition 2.2.** A pomset with preconditions is a tuple $(E, \leq, \lambda)$, such that

- $E$ is a set of events,
- $\leq \subseteq (E \times E)$ is a partial order,
- $\lambda : E \rightarrow (\Phi \times A)$ is a labeling, from which we derive functions $\Phi : E \rightarrow \Phi$ and $A : E \rightarrow A$,
- $\land \Phi(e)$ is satisfiable (consistency), and
- if $d \leq e$ then $\Phi(e)$ implies $\Phi(d)$ (causal strengthening).

We write pairs in $(\Phi \times A)$ as $(\phi \mid a)$, eliding $\phi$ when it is a tautology. We write $d < e$ when $d \leq e$ and $d \neq e$. We often elide explicit universal quantifiers in phrases such as “for all $d$ and $e$ in $E$, if $d \leq e$ then $\Phi(e)$ implies $\Phi(d)$.” We lift terminology and notation from actions and formulae to events. For example, we may say that $e$ is a read when $A(e)$ is a read.

A pomset is completed if it contains a unique termination action, ordered after all other events. Note that, by causal strengthening, the precondition of the termination event of a completed pomset must imply the preconditions of all other events.
The semantics of programs is given as sets of completed pomsets that are closed with respect to downsets, which are similar to prefixes for strings, to augmentation, which may add order, and to implication, which may strengthen formulae.

**Definition 2.3.** $P'$ is a downset of $P$ if $E \supseteq E' \supseteq \{d \in E | \exists e \in E', d \leq e\}$, $\leq' = \leq|_{E'}$, and $\lambda' = \lambda|_{E'}$. We say that $P'$ is an augment of $P$ if $E' = E$, $\lambda' = \lambda$, and $\leq' \supseteq \leq$. We say that $P'$ implies $P$ if $E' = E$, $\leq' = \leq$, $A' = A$, and $\Phi'(e)$ implies $\Phi(e)$.

In examples, we draw pomsets that are augmentation-minimal and implication-minimal. We systematically elide the termination event in diagrams, unless it is relevant to the discussion.

### 2.3 Example Language

We define the language by prefixing individual reads and writes.

$$C, D ::= \text{skip} | r := M; C | r := x^\mu; C | x^\mu := M; C$$

$$| C \parallel D | \text{var } x; C | \text{if}(M)\{C\}\text{else }\{D\}$$

We use common syntax sugar, such as extended expressions, $\overline{M}$, which include memory locations. For example, if $\overline{M}$ includes a single occurrence of $x$, then $y := \overline{M}; C$ is shorthand for $r := x$; $y := M[r/x]; C$. Each occurrence of $x$ in an extended expression corresponds to an separate read.

We write $\text{if}(M)\{C\}$ as shorthand for $\text{if}(M)\{C\}\text{else }\{\text{skip}\}$ and $\text{if}(M)\{C_1\}\{C_2\}; D$ as shorthand for $\text{if}(M)\{C_1; D\}\text{else }\{C_2; D\}$.

The semantic function $[-]$ takes a command and yields a set of pomsets, ranged over by $P$.

### 2.4 Composition

Parallel composition is roughly pomset union, allowing that some events may coalesce, with the resulting precondition being the disjunction of the precondition taken from the two sides. Composition is used to define conditionals (as in [Disselkoen et al. 2019]). We also use it to define address calculation ($\S5$).

Because of consistency (Def. 2.2), we do not include events with contradictory preconditions:

$$\text{if}(r < 0)\{y := 1\}; \text{if}(r \geq 0)\{y := 1\}$$

The parallel composition of these programs includes pomsets with either one of the two events, but not both: including both would violate consistency. However, events with the same label may coalesce, taking the disjunction of their preconditions. Thus, the semantics of the combined program also includes $(r < 0 \lor r \geq 0 \mid Wy1)$. As discussed in the next subsection, coalesced events inherit order from both sides.

**Definition 2.4.** Let $P' \in (P_1 \parallel P_2)$ when there are $P_1 \in P^1$ and $P_2 \in P^2$ such that $P_1$ is completed exactly when $P_2$ is completed, there is at most one termination in $E'$, $E' = E_1 \cup E_2$, $\leq' \supseteq \leq_1 \cup \leq_2$, and for all $e \in E'$, either:

- $A'(e) = A_1(e) = A_2(e)$ and $\Phi'(e)$ implies $\Phi_1(e) \lor \Phi_2(e)$,
- $e \notin E_2$, $A'(e) = A_1(e)$ and $\Phi'(e)$ implies $\Phi_1(e)$, or
- $e \notin E_1$, $A'(e) = A_2(e)$ and $\Phi'(e)$ implies $\Phi_2(e)$.

We then define:

$$[C \parallel D] \triangleq [C] \parallel [D]$$

The definition requires that if $P' \in (P_1 \parallel P_2)$ is completed, then both $P_1$ and $P_2$ are completed, and further, the termination events must coalesce in $P'$. 

2.5 Conditional, Register Assignment, and Skip

Conditional execution is defined using parallel composition and filtering: \((\phi \triangleright P)\) selects the subset of pomsets in \(P\) whose preconditions all imply \(\phi\). Register assignment is defined using substitution: \((P\sigma)\) performs the substitution \(\sigma\) on every formula in \(P\). The semantics of skip is defined using singleton pomsets with label \(\checkmark\).

Definition 2.5. Let \((\phi \triangleright P)\) be the set \(P' \subseteq P\) such that \(P' \in P'\) when \(\Phi(e')\) implies \(\phi (\forall e' \in E')\). Let \((P\sigma)\) be the set \(P'\) where \(P' \in P'\) when there is \(P \in P\) such that: \(E' = E, \leq' = \leq, A' = A, \) and \(\Phi' (e) = \Phi(e)\sigma\). Let \(P \in \text{SKIP}\) when \(E\) has one element labelled with action \(\checkmark\). We then define:

\[
\begin{align*}
[\text{if}(M)\{C\} \text{else } \{D\}] & \hat{=} (M \triangleright [C]) \parallel (\neg M \triangleright [D]) \quad [r := M; C] \hat{=} [C][M/r] \quad [\text{skip}] \hat{=} \text{SKIP}
\end{align*}
\]

Substitution applies to formulae, not actions. For example, \(\langle x=1 | Wx2 \rangle[0/x] = (0=1 | Wx2)\).

As an example of the conditional, consider the following fragments:

\[
\begin{align*}
\text{if}(s)\{x:=1; x:=2\} & \quad \text{if}(\neg s)\{x:=1; x:=3\}
\end{align*}
\]

Putting these together, we can coalesce the \((Wx1)\) events:

\[
\begin{align*}
(C_{\text{cond}} &= \text{if}(s)\{x:=1; x:=2\} \text{else } \{x:=1; x:=3\})
\end{align*}
\]

Let us focus on the left pomset above. It is derived from the composition:

\[
\begin{align*}
s | Wx1 & \xrightarrow{s | Wx2} s | \checkmark \quad \neg s | Wx1 & \xrightarrow{\neg s | Wx3} \neg s | \checkmark
\end{align*}
\]

The existence of the singleton \((\neg s | Wx1)\) is guaranteed by downset closure on \((\ddagger)\). Consistency prevents any pomset in the above \([C_{\text{cond}}]\) from containing both \((Wx2)\) and \((Wx3)\).

Note that the definitions of consistency, downset, and composition prevent the coalescing of \((Wy3)\) in \([\text{if}(s)\{y:=1; y:=3\} \text{else } \{y:=2; y:=3\}]\). Any pomset that included \((Wy3)\) would need to contain both \((s | Wy1)\) and \((\neg s | Wy2)\), which violates consistency.

2.6 Prefixing

Prefixing adds a new read or write event to the beginning of a pomset. As for composition, we allow coalescing. The candidate definition given here fails to validate some compiler optimizations. We give the final definition in §4.

Maintaining downset closure complicates the definition in uninteresting ways; therefore, we perform this closure explicitly. Let \(\nabla P = \{P' | P' \text{ is a downset of some } P \in P\}\).

Candidate 2.6. Let \((\phi | a) \Rightarrow P\) be the set \(\nabla P'\) where \(P' \in P'\) when there is \(P \in P\) such that:

\(\begin{align*}
(p1) E' &= E \cup \{d\}, \\
(p2) \leq' &\supseteq \leq, \\
(p3A) A'(d) &= a, \\
(p3B) A'(e) &= A(e), \\
(p4A) \Phi'(d) &\text{ implies } \phi, \\
(p4B) \text{ if } d \text{ reads } v \text{ from } x \text{ then } \Phi'(e) &\text{ implies } \Phi(e)[v/x], \\
(p4C) \text{ if } d \text{ does not read then } \Phi'(e) &\text{ implies } \Phi(e), \\
(p5A) \text{ if } e \text{ writes then either } d <' e \text{ or } \Phi'(e) &\text{ implies } \Phi(e), \\
(p5B) \text{ if } d \text{ and } e \text{ are actions in conflict, then } d <' e, \\
(p5C) \text{ if } d \text{ is an acquire or } e \text{ is a release, then } d <' e, \text{ and} \\
(p5D) \text{ if } d \text{ is an SC write and } e \text{ is an SC read, then } d <' e.
\end{align*}\)

We then define:

\[
\begin{align*}
[r := x^h; C] &\hat{=} \bigcup_v (R^hxv) \Rightarrow [C][x/r] \\
[x^h := M; C] &\hat{=} \bigcup_v (M = v | W^hxv) \Rightarrow [C][M/x]
\end{align*}
\]
The main work happens in the definition of prefixing (⇒). p1 introduces a new event. p2 ensures that no order is removed from old events. p3 specifies the actions labelling the events. p4 specifies the preconditions (along with p5a). p5 specifies the preserved program order.

The semantics of read and write introduce a separate pomset for each possible value read or written. The value is fixed in each pomset. For writes, the dependence on M appears in the precondition (M = v). This precondition must be satisfied using the substitutions in the semantic rules and p4b. Whereas writes introduce a precondition that must be satisfied sequentially, reads introduce a fulfillment requirement (§2.7) that must be satisfied concurrently.

The possibilities for fulfillment are limited by the program order that is preserved by p5. Requirement p5a connects the sequential semantics of write to the concurrent semantics of read; it imposes the order required by acquire and release actions.

We explain the concurrent semantics in the next section using standard litmus tests. In this subsection, we focus on the sequential semantics. Let us revisit (**):

\[
y := 0; x := 0; (y := x \parallel r := y; \text{if}(r)\{x := r; z := r\} \text{else} \{x := 1\})
\]

It is immediate from the definition that \([x := r; z := r]\) contains pomset candidates such as:

\[
\begin{align*}
& r = 0 \mid Wx \quad r = 0 \mid Wz \\
& r = 1 \mid Wx \quad r = 1 \mid Wz \\
& r = 0 \mid Wx \quad r = 1 \mid Wz
\end{align*}
\]

Consistency (Def. 2.2) rules out the rightmost pomset, since the conjunction of preconditions is unsatisfiable. No order is required between the writes. Combining the middle pomset with \((r = 0 \mid Wx1),\) the conditional \([\text{if}(r)\{x := r; z := r\} \text{else} \{x := 1\}]\) contains:

\[
\begin{align*}
& r = 1 \lor r = 0 \mid Wx1 \\
& r = 1 \mid Wz1
\end{align*}
\]

When prefixing \(r := y,\) we first substitute \([y/r],\) resulting in:

\[
\begin{align*}
& y = 1 \lor y = 0 \mid Wx1 \\
& y = 1 \mid Wz1
\end{align*}
\]

Adding the read action, \([r := y; \text{if}(r)\{x := r; z := r\} \text{else} \{x := 1\}]\) contains:

\[
\begin{align*}
& (y = 1 \lor y = 0) \land (1 = 1 \lor 1 = 0) \mid Wx1 \\
& (y = 1) \land (1 = 1) \mid Wz1
\end{align*}
\]

The second conjunct in each event is required by p4b. p4b also prevents inconsistent reads such as:

\[
\begin{align*}
& (y = 1 \lor y = 0) \land (2 = 1 \lor 2 = 0) \mid Wx1 \\
& (y = 1) \land (1 = 1) \mid Wz1
\end{align*}
\]

p4b also allows predicates to weaken, in which case p5a requires order:

\[
\begin{align*}
& (y = 1 \lor y = 0) \land (1 = 1 \lor 1 = 0) \mid Wx1 \\
& (1 = 1) \land (1 = 1) \mid Wz1
\end{align*}
\]

Adding the write, \([y := 0; r := y; \text{if}(r)\{x := r; z := r\} \text{else} \{x := 1\}]\) substitutes \([0/y],\) resulting in:

\[
\begin{align*}
& (0 = 0 \mid Wy) \quad (0 = 1 \lor 0 = 0) \land (1 = 1 \lor 1 = 0) \mid Wx1 \\
& (1 = 1) \land (1 = 1) \mid Wz1
\end{align*}
\]

Simplifying the tautologies, we have:

\[
\begin{align*}
& Wy0 \quad Wy1 \\
& Wx1 \quad Wz1
\end{align*}
\]
As discussed at the beginning of this section, an attempt to replicate this execution with (†) fails:

\[
y := 0; x := 0; (y := x \parallel r := y; \text{if}(r)\{x := r; z := r\} \text{else}\{x := 2\})
\]

\(W_0\) \(\xrightarrow{}\) \(W_0\) \(\xrightarrow{}\) \(R_1\) \(\xrightarrow{}\) \(W_1\) \(\xrightarrow{}\) \(W_1\) \(\xrightarrow{}\) \(W_1\) \(\xrightarrow{}\) \(W_1\) \(\xrightarrow{}\) \(W_1\) \(\xrightarrow{}\) \(\\)

\[(†)\]

The difference between (**) and (†) can be seen in the conditional \([\text{if}(r)\{x := r; z := r\} \text{else}\{x := 2\}]\), which contains:

- \(r = 1 \mid W_1\)
- \(r = 1 \mid W_1\)
- \(r = 2 \lor r = 0 \mid W_2\)
- \(r = 2 \mid W_2\)

However, there is no pomset that contains \((r = 1 \lor r = 0 \mid W_1)\). Using the left pomset above, it is only possible to satisfy the precondition of \((r = 1 \mid W_1)\) using \(p_{4b}\) when prefixing \((R_1)\). This forces a dependency between the read and write via \(p_{5a}\).

### 2.7 Fulfillment, Local Declarations, and Top-Level Pomsets

At the point that \(x\) is bound, we require that every read of \(x\) be fulfilled. Fulfillment plays the role that reads-from and coherence play in other relaxed memory models, yet it is not the same.

**Definition 2.7.** Two actions conflict if one writes a location and the other either reads or writes the same location. We say \(d\) fulfills \(e\) (on \(x\)) if \((f_1)\) \(d\) writes \(v\) to \(x\), \((f_2)\) \(e\) reads \(v\) from \(x\), \((f_3)\) \(d < e\), and \((f_4)\) for every conflicting write \(c\), either \(c \leq d\) or \(e \leq c\).

\(f_3\) requires that a write \(d\) is ordered before any read \(e\) that it fulfills; this order is typically called reads from. \(f_4\) requires that any conflicting write \(c\) is ordered before \(d\) or after \(e\); this order is typically called extended coherence. For readability, we draw the order required by \(f_3\) using bold green arrows and the order required by \(f_4\) using dashed red arrows. As an example, consider:

\[
x := 1 \parallel x := 2 \parallel x := 3 \parallel x := 4 \parallel x := 5 \parallel r := x; r := x; r := x; r := x; r := x
\]

\((\text{co1})\)

A write is relevant if it is read from. In order to fulfill all of the reads on \(x\) in the example, we pick a total order on the relevant writes: in this case, \((W_1) \leq (W_2) \leq (W_5)\). The reads slot between these, immediately after their fulfilling write. Reads are not necessarily ordered with respect to each other, even if they come from the same thread, as do the reads here. Irrelevant writes also float relative to each other, as do \((W_3)\) and \((W_4)\). But irrelevant writes must be ordered with respect to relevant writes and reads. The resulting order is somewhat weaker than traditional extended coherence, which requires a total order on the writes, regardless of whether they are relevant. We discuss coherence further in §3.1.

In order to be \(x\)-closed, a pomset must be “done” with \(x\), in both the concurrent and the sequential semantics. The concurrent semantics requires that all reads of \(x\) be fulfilled. The sequential semantics requires that all formulae be independent of \(x\) (Def. 2.1): \(\forall \phi. \phi \equiv \phi[v/x] \equiv \phi\).

**Definition 2.8.** A pomset is \(x\)-closed if every read on \(x\) is fulfilled, and every formula is independent of \(x\). Let \((\mathcal{V}x.\mathcal{P})\) be \(\mathcal{P}' \subseteq \mathcal{P}\) such that \(\mathcal{P}' \in \mathcal{P}\) when \(\mathcal{P}'\) is \(x\)-closed. We define:

\[
\text{[}\text{var } x; C\text{]} \triangleq \text{[} \mathcal{V}x.\mathcal{P}\text{]} \text{[} C\text{]}
\]

A pomset is top-level if it is \(x\)-closed for every location \(x\).
Together with \( f4 \), the definition of \( x \)-closed disallows the following execution:
\[
\begin{align*}
\text{var } x; & \quad (x := 1; y_1 := 1) \parallel \text{if}(z_1)(x := 2); y_2 := 1 \parallel r := z_2; s := x) \\
(Wx1) & \rightarrow (W^a y_1); Rz1 \rightarrow Wx2 \rightarrow W^a y_2 \rightarrow R^a z_2 \rightarrow Rx1 \\
(\uparrow\uparrow)
\end{align*}
\]
In order to close \( x \), we must choose whether \((Wx2)\) is preceding \((Wx2 \rightarrow Wx1)\) or following \((Rx1 \rightarrow Wx2)\). This prevents \((Wx2)\) from blocking the read after parallel composition. For example, if \((\uparrow\uparrow)\) were placed in the context \( b := a \parallel d := c \parallel [-] \), we would have:
\[
(Wx1) \rightarrow (W^a y_1) \rightarrow Ry1 \rightarrow Wz1 \rightarrow Rz1 \rightarrow Wx2 \rightarrow W^a y_2 \rightarrow Ry2 \rightarrow Wz2 \rightarrow R^a z_2 \rightarrow Rx1 \\
\]
This violates the conventional, weaker statement of \( f4 \): there is no conflicting write \( c \) such that \( d < c < e \). By requiring order on \((Wx2)\) we forbid this blocker and validate scope extrusion (§3.2).

### 3 PROPERTIES OF THE BASIC MODEL

It is amazing how much the semantics of §2 “gets right” out of the box, including value range analysis, internal reads, and SC access, all of which can be complex in other models. In this section, we walk through several litmus tests, valid rewrites and invalid rewrites. The examples show that \( p5a \rightarrow p5d \) and \( f3 \rightarrow f4 \) are understandable as general principles. The interaction of these principles is limited to a single, global, pomset order. We discuss tweaks to the semantics in §4.

#### 3.1 Litmus Tests

Pugh [2004] developed a set of litmus tests for the java memory model. Our model gives the expected result for all but cases 16, 19 and 20 (unrolling loops): we discuss \( tc16 \) below; \( TC19 \) and \( TC20 \) involve a thread join operation, which is not expressible in our language. Our model also agrees with the oota examples of Batty et al. [2015, §4] and the “surprising and controversial behaviors” of Manson et al. [2005, §8]. See Paviotti et al. [2020] for an exhaustive list of litmus tests.

**Buffering.** Consider the store buffering and load buffering litmus tests:
\[
\begin{align*}
\text{Buffering. Consider the store buffering and load buffering litmus tests:} \\
(Wx0) & \rightarrow Wx1 \rightarrow Wy0 \rightarrow Wy1 \rightarrow Rx0 \rightarrow Rx1 \rightarrow Wy1 \\
& \quad (sb/lb)
\end{align*}
\]
Because there are no intra-thread dependencies, the desired outcomes are allowed, as shown.

**Publication.** \( f3 \rightarrow f4 \) and \( p5b \rightarrow p5c \) ensure correct publication, prohibiting stale reads:
\[
\begin{align*}
\text{Publication. } f3 \rightarrow f4 \text{ and } p5b \rightarrow p5c \text{ ensure correct publication, prohibiting stale reads:} \\
(Wx0) & \rightarrow Wx1 \rightarrow W^a y_1 \rightarrow R^a y_1 \rightarrow Rx0 \\
& \quad (pub1)
\end{align*}
\]
This pomset is disallowed, since \((Rx0)\) fails to satisfy \( f4 \): \((Wx0) < (Wx1) < (Rx0)\). Attempting to satisfy this requirement, one might order \((Rx0)\) before \((Wx1)\), but this would create a cycle.

**Coherence.** Our model of coherence does not correspond to either Java or C11. We have chosen the model to validate \( \text{cse} \) (unlike C11 relaxed atomics) and the local \( \text{sc-drf} \) theorem (unlike Java).

Since reads are not ordered by \( p5b \), we allow the following unintuitive behavior. C11 includes read-read coherence between relaxed atomics in order to forbid this:
\[
\begin{align*}
\text{Coherence. Our model of coherence does not correspond to either Java or C11. We have chosen} \\
\text{the model to validate } \text{cse} \text{ (unlike C11 relaxed atomics) and the local } \text{sc-drf} \text{ theorem (unlike Java).} \\
\text{Since reads are not ordered by } p5b, \text{ we allow the following unintuitive behavior. C11 includes} \\
\text{read-read coherence between relaxed atomics in order to forbid this:} \\
x := 1; x := 2 \parallel y := x; z := x \\
(Wx1) \rightarrow Wx2 \rightarrow Rx2 \rightarrow W^a y_2 \rightarrow Rx1 \rightarrow Wz1 \\
& \quad (co2)
\end{align*}
\]
Here, the reader sees \( 2 \) then \( 1 \), although they are written in the reverse order. This behavior is allowed by Java in order to validate \( \text{cse} \).
However, our model is more coherent than Java, which permits the following:

\[
\begin{align*}
    r & := x; x := 1 & s & := x; x := 2 \\
    R_{x2} & \rightarrow \triangleleft W_{x1} & R_{x1} & \rightarrow \triangleleft W_{x2}
\end{align*}
\]  

(TC16)

We also forbid the following, which Java allows:

\[
\begin{align*}
    x & := 1; y^{ra} := 1 & x & := 2; z^{ra} := 1 & r & := z^{ra}; r & := y^{ra}; r & := x; r & := x \\
    W_{x1} & \rightarrow \triangleleft W_{y^{ra}1} & W_{x2} & \rightarrow \triangleleft W_{z^{ra}1} & R_{y^{ra}1} & \rightarrow \triangleleft R_{z^{ra}1} & R_{x2} & \rightarrow \triangleleft R_{x1}
\end{align*}
\]  

(CO3)

The order from \((R_{x1})\) to \((W_{x2})\) is required to fulfill \((R_{x1})\). The outcome is disallowed due to the cycle. If this outcome were allowed, then racing writes would be visible, even after a full synchronization; this would invalidate local reasoning about data races (§8).

\textbf{MCA.} We present a few examples that are hallmarks of \textit{MCA} architectures.

\[
\begin{align*}
    \text{if}(z)\{x := 0\} & ; x := 1 & \text{if}(y)\{z := 0\} & ; z := 1 & \text{if}(x)\{y := 0\} & ; y := 1 \\
    R_{z1} & \rightarrow \triangleleft W_{x0} & R_{x1} & \rightarrow \triangleleft W_{y0} & R_{y1} & \rightarrow \triangleleft W_{z0} & W_{z1}
\end{align*}
\]  

(MCA1)

These candidate executions are invalid, due to cycles. \textit{MCA1} is an example of \textit{write subsumption} [Pulte et al. 2018, §3]. In \textit{MCA2}, \((W_{x1})\) is delivered to the second thread, but not the third; this is similar to the well know \textit{IRIW} (Independent Reads of Independent Writes) litmus test, which is also disallowed by \textit{MCA} architectures if the reads within each thread are ordered.

If \(y^{ra}\) is changed to \(y^{rlx}\) in \textit{MCA2}, then there would be no order from \((R_{rlx}y1)\) to \((R_{x0})\), and the execution would be allowed. Since read-read dependencies do not appear in pomset order, the execution would still be allowed if a control or address dependency were to be introduced between the reads. See example \textit{ADDR} (§10) for further discussion.

\textit{Internal Reads and Value Range Analysis.} The JMM causality test cases [Pugh 2004] are justified via compiler analysis, possibly in collusion with the scheduler: If every observed value can be shown to satisfy a precondition, then the precondition can be dropped. For example, \textit{TC1} determines that the following execution should be allowed, as it is in our model:

\[
\begin{align*}
    x & := 0; (r := x; \text{if}(r \geq 0)\{y := 1\}) & x := y \\
    W_{x0} & = \triangleleft R_{x1} & 0 \geq 0 \rightarrow W_{y1} & \rightarrow R_{y1} & \rightarrow W_{x1}
\end{align*}
\]  

(TC1)

In this example, \((W_{x0})\) “fulfills” the read of \(x\) that is used in the guard of the conditional. This is possible when prefixing \((R_{x1})\) performs the substitution \([x/r]\), but does not weaken the resulting precondition \((x \geq 0 \mid W_{y1})\). Subsequently prefixing \((W_{x0})\) substitutes \([0/x]\), resulting in the tautological precondition \((0 \geq 0 \mid W_{y1})\). Note that the execution does not have an action \((R_{x0})\).

Our semantics is robust with respect to the introduction of concurrent writes, as in \textit{TC9}:

\[
\begin{align*}
    x & := 0; (r := x; \text{if}(r \geq 0)\{y := 1\}) & x := y & x := -2 \\
    W_{x0} & \rightarrow \triangleleft R_{x1} & 0 \geq 0 \rightarrow W_{y1} & \rightarrow R_{y1} & \rightarrow W_{x1} & \rightarrow W_{x-2}
\end{align*}
\]  

(TC9)

The calculation of this pomset is unchanged from \textit{TC1}.

Examples such as \textit{TC9} present substantial difficulties in other models. When thought of in terms of compiler optimizations, \textit{TC9} is justified by global value analysis in collusion with the thread
scheduler. This execution is disallowed by our event structure model [Jeffrey and Riely 2016]. It is allowed by Pichon-Pharabod and Sewell [2016], at the cost of introducing dead reads.

The reasoning for tc2 is similar, but in this case no value is necessary to satisfy the precondition:

\[
\text{tc2: } r := x; s := x; \text{ if}(r=s)\{y := 1\} \parallel x := y
\]

Note that in \([s := x; \text{ if}(r=s)\{y := 1\}]\), the precondition on \((Wy1)\) must imply \((r=x \land r=1)\). The first is imposed by p5A, the second by p4B, ensuring that the two reads see the same value.

Using arm8 terminology, these executions involve internal reads, which are fulfilled by a sequentially preceding write. Read actions always generate an event that must be fulfilled, and therefore cannot be ignored, even if they are unused. This fact prevents internal reads from ignoring concurrent blocking writes.

\[
\text{INTERNAL1: } x := 1; \ a^{\text{ra}} := 1; \ \text{if}(z^{\text{ra}})\{y := x\} \parallel \text{if}(a^{\text{ra}})\{x := 2; z^{\text{ra}} := 1\}
\]

Here, \((Wx1)\) violates f4. The precondition \((1=1)\) is imposed by p4B. The pomset becomes inconsistent if we change \((Rx1)\) to \((Rx2)\), since the precondition would change to \((2=1)\).

Internal reads are notoriously difficult to get right. Consider [Podkopaev et al. 2019, Ex 3.6]:

\[
\text{INTERNAL2: } r := x; \ y^{\text{ra}} := 1; s := y; z := s \parallel x := z
\]

This behavior is allowed in our model, as it is in arm8. Note that \([z := s]\) includes \((s=1 \mid Wz1)\). Prepending a read, \([s := y; z := s]\) may update the precondition to \((y=1 \mid Wz1)\) without introducing order. Further prepending \((W^{\text{ra}}y1)\) results in \((1=1 \mid Wz1)\).

Our model drops order into actions that depend on a read that can be fulfilled internally, by a prefixed write. This is natural consequence of substitution. The arm8 model has to jump through some hoops to ensure that internal reads are handled correctly. arm8 takes the symmetric approach: rather than dropping order out of an internal read, arm8 drops the order into it. This difference complicates the proof for arm8 (§7).

SC access. p5d ensures that program order between SC operations is always preserved. Combined with F3–F4, this is sufficient to establish that programs with only SC access have only SC executions; for example, the executions of SB/LB are banned when the actions of the two threads are all SC. It is also immediate that SC actions can be totally ordered, using any linearization of pomset order. Just as SC access in arm8 is simplified by mca, it is simplified here by the global pomset order.

SC access is not as strict as volatile access in Java. For example, our model allows the following, since there is no order from \((W^{\text{sc}}x2)\) to \((Wy1)\)—recall that SC writes are releases.

\[
\text{sc1: } r := y; x^{\text{sc}} := 1; s := x \parallel x^{\text{sc}} := 2; y := 1
\]

This execution is disallowed by Dolan et al. [2018, §8.2], preventing them from using stlr to implement volatile writes on arm8. Our implementation strategy does use stlr for SC writes, as is standard. For further discussion, see examples PAST and FUTURE in §8.
Watt et al. [2020, §3.1] noticed a similar difficulty in Javascript [ECMA International 2019, §27]:

\[
x^{SC} := 1; r := y^{SC} \parallel y^{SC} := 1; y^{SC} := 2; x := 2; s := x^{SC}
\]

This execution is allowed both by our semantics and by ARM8 (using stlr for SC writes and ldar for SC reads). However, it is not allowed by Javascript 2019. In Javascript, the rules relating SC and relaxed access are subtle. As result of these interactions, Javascript 2019 fails to satisfy sc-drf [Watt et al. 2019]. The rules are even more complex in C11; see sc3 and sc4 in §5 for a discussion of SC fences in C11. In our model, only p5d is required to explain SC access.

### 3.2 Valid and Invalid Rewrites

When \([C] \supseteq \[C']\), we say that \(C'\) is a valid transformation of \(C\). In this subsection, we show the validity of specific optimizations. Let id\((C)\) be the set of locations and registers that occur in \(C\).

The semantics validates many peephole optimizations. Most apply only to relaxed access.

\[
[x := M; y := N; C] = [y := N; x := M; C] \quad \text{if } x \neq y \quad \text{(ww)}
\]

\[
[r := x; y := N; C] = [y := N; r := x; C] \quad \text{if } \text{id}(r := x) \cap \text{id}(y := N) = \emptyset \quad \text{(rw)}
\]

\[
[r := x; s := y; C] = [s := y; r := x; C] \quad \text{if } r \neq s \quad \text{(rr)}
\]

The independent reorderings (ww, rw and rr) follow from p5, since no order is imposed. p5 also validates roach-motel reorderings [Sevčík 2008]. For example, the rules for relaxed writes are:

\[
[x := M; r := y^a; C] \supseteq [r := y^a; x := M; C] \quad \text{if } x \neq y \quad \text{(roach1)}
\]

\[
[y^a := N; x := M; C] \supseteq [x := M; y^a := N; C] \quad \text{if } x \neq y \quad \text{(roach2)}
\]

Relaxed reads are similar. Redundant load elimination (rl) follows from p1, taking \(d \in E\).

\[
[r := x^d; s := r; C] \supseteq [r := x^d; s := r; C] \quad \text{(rl)}
\]

RL holds regardless of the access mode. Since p5b does not impose order between reads of the same location, RR can allow the possibility that \(x = y\). As a result, read optimizations are not limited by the power of aliasing analysis. By composing RR and RL, we validate cse:

\[
[r_1 := x; s := y; r_2 := x; C] \supseteq [r_1 := x; r_2 := r_1; s := y; C] \quad \text{if } r_2 \neq s \quad \text{(cse)}
\]

Many laws hold for the conditional, such as dead code elimination (dc) and code lifting (cl):

\[
[\text{if}(M)\{C\} \text{ else } \{D\}] = [C] \quad \text{if } M \text{ is a tautology} \quad \text{(dc)}
\]

\[
[\text{if}(M)\{C\} \text{ else } \{C\}] \supseteq [C] \quad \text{(cl)}
\]

Code lifting also applies to program fragments inside a conditional. For example:

\[
[\text{if}(M)\{x := N; C\} \text{ else } \{x := N; D\}] \supseteq [x := N; \text{if}(M)\{C\} \text{ else } \{D\}] 
\]

We discuss the inverse of cl in §4.

As expected, parallel composition commutes with conditionals and declarations, and conditionals and declarations commute with each other. For example, we have scope extrusion [Milner 1999]:

\[
[C \parallel \text{var } x; D] = [\text{var } x; (C \parallel D)] \quad \text{if } x \notin \text{id}(C) \quad \text{(se)}
\]
Invalid Rewrites. The definition of location binding does not validate renaming of locations: if \( x \neq y \) then \([\text{var } y; C] \neq [\text{var } x; C[x/y]]\), even if \( C \) does not mention \( x \). This is consistent with support for address calculation, which is required by realistic memory allocators.

INTERNAL2 shows that—like most relaxed models—our model fails to validate thread inlining. The given execution is impossible if the first thread is split, as in \([r := x; y^a := 1 \parallel s := y; z := s \parallel x := z]\). The write in the first thread cannot discharge the precondition in the second, now separate.

Some rewrites are invalid in a concurrent setting, such as relevant read introduction:

\[
[r := x; \text{if}(r \neq r)(y := 1)] \not\models [r := x; s := x; \text{if}(r \neq s)(y := 1)]
\]

Observationally, these are distinguished by the context \([-] \parallel x := 1 \parallel x := 2\).

Similarly, redundant write after read elimination is invalid [Sevčík 2008, §5.3-4]:

\[
[r := x; x := r; s := x; \text{if}(r \neq r)(y := 1)] \not\models [r := x; s := x; \text{if}(r \neq r)(y := 1)]
\]

These are distinguished by the context \(x := 1; a^a := 1 \parallel x := 2; z^a := 1 \parallel \text{if}(a^a \land z^a)\{-\}\).

Write introduction is also invalid, even when duplicating an existing write:

\[
[x := 1] \not\models [x := 1; x := 1]
\]

These are distinguished by the context: \([-] \parallel r := x; x := 2; s := x; \text{if}(r = s)(z := 1)\).

4 CASE ANALYSIS, ACCESS ELIMINATION, AND READ INTRODUCTION

The previous section shows the simplicity and beauty of pomsets with preconditions as a model of relaxed memory. In this section we look at some of the complications and ugliness.

We limit attention to relaxed access—Candidate 2.6 provides our final definition of prefixing for ra/sc access. In particular, we do not attempt to validate rewrites that eliminate ra/sc accesses, beyond those already given.

For relaxed access, the following definition enriches Candidate 2.6 with additional pomsets. As we discuss below, this definition validates read elimination (RE), store forwarding (SF), dead store elimination (DS), and case analysis (CA). We end this section with a brief discussion of a read-enriched semantics that validates irrelevant read introduction (RI).

In this section, we elide \(\text{rlx}\)-mode annotations in definitions.

Definition 4.1. Let \((\phi \mid a) \Rightarrow \mathcal{P}\) be the set \(\nabla \mathcal{P}'\) where \(\mathcal{P}' \in \mathcal{P}'\) when there is some \(P \in \mathcal{P}\) that satisfies P1-P5 of Candidate 2.6 such that:

- (p6) if \(d\) is a release, \(e_1\) is an acquire, \(e_1 \leq e_2\), then \(\Phi(e_2)\) is location independent.

Let \(\text{weaken}_{\text{Rx}}(\mathcal{P})\) be the set \(\mathcal{P}'\) where \(\mathcal{P}' \in \mathcal{P}'\) when there is \(P \in \mathcal{P}\) such that: \(E' = E, \leq' = \leq\), \(\mathcal{A}' = \mathcal{A}\), and either \(\Phi'(e)\) implies \(\Phi(e)\) or \(e\) is \(\leq\)-minimal and \(\mathcal{A}(e) = \text{Rxv}\).

Let \(\text{weaken}_{\text{Rx}}(\mathcal{P}) = \bigcup_\circ \text{weaken}_{\text{Rxw}}(\mathcal{P})\).

Let \(\text{weaken}_{\text{Rx,M}}(\mathcal{P})\) be the set \(\mathcal{P}'\) where \(\mathcal{P}' \in \mathcal{P}'\) when there is \(P \in \mathcal{P}\) such that: \(E' = E, \leq' = \leq\), \(\mathcal{A}' = \mathcal{A}\), and either \(\Phi'(e)\) implies \(\Phi(e)\) or \(e\) is \(\leq\)-minimal, \(\mathcal{A}(e) = \text{Rxv}\), and \(\Phi'(e)\) implies \(M = v \lor \Phi(e)\).

Let \(\text{cover}_{\text{s}}(\mathcal{P})\) be the set \(\mathcal{P}'\) such that \(\mathcal{P}' \in \mathcal{P}'\) when for every release \(e' \in E'\), there is some \(d' \in E'\) such that \(d' \leq e'\) and \(d'\) writes \(x\).

\[
[r := x; C] \overset{\text{weaken}_{\text{Rx}}(C)}{\Rightarrow} \bigcup_\circ (\text{Rxv}) \Rightarrow \text{weaken}_{\text{Rxw}}(C)[x/r] \quad [x := M; C] \overset{\text{weaken}_{\text{Rx,M}}(\text{cover}_{\text{s}}(C)[M/x])}{\Rightarrow} \bigcup_\circ (M = v \mid \text{Wxv}) \Rightarrow [C][M/x]
\]

\(^2e\) is \(\leq\)-minimal if there is no \(d\) such that \(d \leq e\).

There are six changes in the definition: To validate read elimination, we include \([C][x/r]\). To ensure that this does not allow stale reads, we add requirement \(p6\) to the definition of prefixing. To validate case analysis on reads actions, we apply weaken\(_{Rxv}\) to \([C][x/r]\) before prefixing. To validate case analysis with eliminated reads, we apply weaken\(_R\) to \([C][x/r]\). To validate write elimination, we include cover\(_x[\text{C}][M/x]\). To validate case analysis with eliminated writes, we apply weaken\(_{Wxy}\).

**Read Elimination and Store Forwarding.** In our work on microarchitecture [Disselkoen et al. 2019], read actions could be observed using cache effects. Candidate 2.6 maintains this perspective—for example, it distinguishes \([r := x]\) and \(\geq [\text{skip}]\) even though there is no context in the language of this paper that can distinguish these programs. If one accepts that these programs should be equated at an architectural level, then one would expect the semantics to validate read elimination (RE) and store forwarding (SF).

\[
\begin{align*}
[r := x; C] & \supseteq [C] & \text{if } r \notin \text{id}(C) \quad & \text{(RE)} \\
[x^\mu := M; r := x; C] & \supseteq [x^\mu := M; r := M; C] \quad & \text{(SF)}
\end{align*}
\]

These optimizations are validated by Definition 4.1, since \([r := x; C] \supseteq [C][x/r]\). The proof of SF also appeals to the definition of write and the definition of register assignment.

Let us revisit the internal read examples from §3.1. With read elimination, the read action (Rx1) can be elided in \text{INTERNAL}2; regardless, the substitution into the write of \(z\) is the same. On a more troubling note, the read action (Rx1) can be also elided in \text{INTERNAL}1, potentially converting this non-execution into a valid execution, violating SC-DRF. The addition of \(p6\) to the definition of prefixing prevents this outcome. When computing \([x := 1; a^r := 1; \text{if}(b^r)(y := x)]\), \(p6\) prevents prefixing \(\text{W}^r\alpha1\) in front of:

\[
\begin{array}{c}
\text{R}^\alpha b1 \rightarrow \text{Rx1} \rightarrow x = 1 | \text{W} y1
\end{array}
\]

In order to satisfy \(p6\), the precondition of \((W y1)\) must be location independent.

**Dead Store Elimination.** Dead store elimination (DS) is symmetric to redundant load elimination.

\[
[x := M; x := N; C] \supseteq [x := N; C] \quad & \text{(DS)}
\]

The rewrite is less general than RE because general store elimination is unsound. For example, “\(x := 0\)” and “\(x := 0; x := 1\)” can be distinguished by the context “[\(\_\)] \| z := x\”.

DS is valid under Definition 4.1. A write may only be removed if it is covered by a following write. This prevents bad executions, such as:

\[
\begin{array}{c}
W x1 \rightarrow W x2 \rightarrow \text{W}^r y1 \rightarrow \text{R}^r y1 \rightarrow \text{Rx1}
\end{array}
\]

In this diagram, we have included a “non-event”—dashed border—to mark the eliminated write. In general, there may need to be many following writes, one for each subsequent release.

**Case Analysis.** Definition 4.1 satisfies disjunction closure.

**Definition 4.2.** We say that \(P\) is a disjunct of \(P'\) and disjunct of \(P''\) when \(E = E' \supseteq E''\), \(\leq = \leq' \supseteq \leq''\), \(\mathcal{A} = \mathcal{A'} \supseteq \mathcal{A''}\), \(\Phi(e)\) implies \(\Phi'(e) \lor \Phi''(e)\) if \(e \in E''\), and \(\Phi(e)\) implies \(\Phi'(e)\) otherwise.

We say that \(P\) is disjunction closed if \(P \in \mathcal{P}\) whenever there are \(\{P', P''\} \subseteq \mathcal{P}\) such that \(P\) is a disjunct of \(P'\) and disjunct of \(P''\).

Disjunction closure is sufficient to establish case analysis (CA):

\[
[C] \supseteq [\text{if}(\text{M})(C) \text{else } \{C\}] \quad & \text{(CA)}
\]
As we discuss below, Candidate 2.6 is not disjunction closed; however, it becomes closed if \texttt{p5B} is strengthened to include read-read coherence, thus sacrificing sacrifice \texttt{cse}. This compromise is considered reasonable for C11 atomics, which are meant to be used sparingly. It is less attractive for relaxed access in safe languages, like Java.

We start the discussion of case analysis with a version of Candidate 2.6 that strengthens \texttt{p5B} to include read-read coherence. We then look at three relaxations in turn: write elimination, reads elimination, and finally dropping read-read coherence. Definition 4.1 performs a bit of disjunctive closure in each case.

Write elimination causes disjunction closure to fail. For example, consider the following executions of $C_W$; the second uses write elimination. (To make coalescing explicit, we show the element of the carrier set $E$ to left of the label.)

$$C_W = x := 1; \texttt{if}(r)\{x := 1\}$$

Using disjunction, $[\texttt{if}(s)\{C_W\} \texttt{else } \{C_W\}]$ includes the singleton $d: (Wx1)$, but $[C_W]$ does not:

In the definition of composition, any actions with the same label and downset can coalesce. Our solution is to weaken the preconditions on writes to the same location when eliminating a write. We do this using the function \texttt{weaken}_{WxM}, which weakens the precondition of any $\texttt{-minimal}$ $(Wx1)$ to $(M = v \lor \phi)$, where $\phi$ is formula before prefixing. When eliminating $(Wx1)$ in front of $(r \mid Wx1)$ in the example above, we arrive at the tautology $(1 = 1 \lor r)$ for the “old” write.

Because the reads are unordered, they can be confused when coalescing, resulting in:

$$\texttt{if}(N)\{C_R\} \texttt{else } \{C_R\}$$

$$\texttt{if}(\neg N)\{C_R\}$$

Because the reads are unordered, they can be confused when coalescing, resulting in:

$$\texttt{if}(N)\{C_R\} \texttt{else } \{C_R\}$$

$$\texttt{if}(\neg N)\{C_R\}$$

which is:

$$d: (N \lor \neg N \land M) \mid R x0 \quad e: (N \land M) \lor \neg N \mid R x0$$

But this pomset does not occur in $[C_R]$. Our solution is to weaken the preconditions on reads so that both $\texttt{f}[C_R]$ and $[\texttt{if}(N)\{C_R\} \texttt{else } \{C_R\}]$ include:

$$d: (R x0) \quad e: (R x0)$$

Note that the precondition on the reads are weaker than one would expect. This is not a problem for reads, since they must also be fulfilled—allowing more reads increases the obligations of fulfillment. The same solution would not work for writes—as we discussed at the end of §3, allowing more writes is simply unsound. Fortunately, this problem does not occur when prefixing a write in front of another write, due to the order required by \texttt{p5B}.

\textbf{Irrelevant Read Introduction.} Compilers sometimes introduce reads in order to lift code. Consider the following example [Sevčík 2008, §1.4.5]:

$$[\texttt{if}(r)\{s := x; y := s\}] \notin [s := x; \texttt{if}(r)\{y := s\}]$$

The right-hand program is derived from the left by introducing an irrelevant read in the else-branch, then moving the common code out of the conditional. Definition 4.1 does \textit{not} validate this rewrite.
Read introduction is only valid "modulo irrelevant reads." We capture this idea using read saturation. Read saturation allows us to add actions of the form (Rxv) to the left-hand side, validating the inclusion.

Let \( \text{read}(P) \) be the set \( P' \) where \( P' \in P \) when \( \exists P \in P \) and \( \exists D \) such that \( E' = E \cup D, \leq' \supseteq \leq, \lambda' \supseteq \lambda \), and \( \forall d \in D \). \( \exists v \cdot \mathcal{A}(d) = (Rxv) \). Note that if \( P' \supseteq P \), then \( \text{read}(P') \supseteq \text{read}(P) \).

Read introduction (RI) is valid under the saturated semantics.

\[
\text{read}[C] \supseteq \text{read}[r := x; C] \quad \text{if } r \notin \text{id}(C) \tag{RI}
\]

With RI, the model satisfies all of the transformations of Sevčík [2008, §5.3-4] except redundant write after read elimination (see §3.2) and reordering with external actions, which we do not model.

5 FENCES, READ-MODIFY-WRITE, AND ADDRESS CALCULATION

We extend the model to include additional features: fences, read-modify-write actions (rmws), and address calculation. The proofs given later in the paper extend to include these features.

Fences. Syntactic fences "\( F_j; C \)" have corresponding actions: \( \{F_j\} \). The syntactic fence mode \( (v := \text{rel} | \text{acq} | \text{sc}) \) is either release, acquire, or sequentially-consistent.

\( F_{\text{rel}} \) is a release. \( F_{\text{acq}} \) is an acquire. \( F_{\text{sc}} \) is both a release and an acquire.

\[
\{F_j; C\} \Rightarrow \{F_j\} \Rightarrow \{C\}
\]

With no further changes, syntactic fences would impose exactly the same order as synchronization actions. This is sufficient to simulate \( \text{sc} \) accesses, since \( \text{sc} \) fences are very strong. However, it is insufficient to simulate \( \text{ra} \) accesses. Thus we add the following to Definition 2.6:

\( p5e \) if \( d \) reads, and \( e \) is an acquiring fence, then \( d \prec e \), and

\( p5f \) if \( d \) is a releasing fence, and \( e \) writes, then \( d \prec e \).

Consider the following variant of PUB1:

\[
\begin{align*}
x := 0; x := 1; F_{\text{rel}}; y := 1 & \parallel r := y; F_{\text{acq}}; s := x
\end{align*}
\]

\( p5f \) requires that \( F_{\text{rel}} \leq (W, y)_1 \). \( p5e \) requires that \( (R, y)_1 \leq (F_{\text{acq}}) \). The other order involving fences is required by \( p5c \). The attempted execution is invalid: the stale read \((R, x)_0\) violates \( p4 \).

As for \( \text{rl} \), redundant fence elimination (RF) follows from \( P1 \), regardless of the access mode.

\[
\{F_j; F_{\mu}; C\} \supseteq \{F_j; C\} \tag{RF}
\]

Our semantics does not suffer from overly weak fencing (sc3) or a lack of fence cumulativity (sc4). The following examples, from Lahav et al. [2017, Figs. 5 and 6], are allowed by both the original C11 and the model of Batty et al. [2016]. We omit 0-initialization in these examples:

\[
\begin{align*}
x := 1 & \parallel r := x; F_{\text{sc}}; r := y & \parallel y := 1; F_{\text{sc}}; r := x
\end{align*}
\]

\( \text{sc3} \)

\[
\begin{align*}
x := 1; z_{\text{ra}} := 1; & \parallel r_{\text{ra}} := z; F_{\text{sc}}; r := y & \parallel y := 1; F_{\text{sc}}; r := x
\end{align*}
\]

\( \text{sc4} \)

The executions are disallowed, due to the evident cycles. While these results are immediate in our model, it is worth noting that they are anything but immediate in the various models of C11.
Read-Modify-Write. We discuss rmw operations that work on a single location in memory, such as fetch-and-add (FADD) and compare-and-swap (CAS). These operations can be modeled using read/write actions or using an additional relation between events. The second approach is more general and less obvious, therefore we explain it here.

In Definition 2.2, we require that a (memory model) pomset be a tuple \((E, \leq, \lambda, \text{rmw})\), where \(\text{rmw} \subseteq \leq\) relates the two events of a successful rmw. Additionally, we require that:

- If \(c, e\) write the same \(x, c \leq e\) and \(d \overset{\text{rmw}}{\rightarrow} e\) then \(c \leq d\).
- If \(c, e\) write the same \(x, d \leq c\) and \(d \overset{\text{rmw}}{\rightarrow} e\) then \(e \leq c\).

Other than these two changes, nothing else changes. In particular, rmws require no special treatment in Definition 2.4: the constituent events of an rmw may coalesce with other events as a result of parallel composition. We elide the obvious and tedious semantic rules that generate \(\text{rmw}\).

This definition ensures atomicity, disallowing executions such as [Podkopaev et al. 2019, Ex. 3.2]:

\[
x' := 0; s := \text{FADD}_{\text{rb}, \text{ra}}(x) \parallel x' := 2; s := x
\]

By using two actions rather than one, the definition allows examples such as the following, which is allowed by ARM8 [Podkopaev et al. 2019, Ex. 3.10]:

\[
r := y; z := r \parallel r := z; x := 0; s := \text{FADD}_{\text{rb}, \text{ra}}(x); y := s + 1
\]

Address Calculation. In the definition of a data model, we require that locations have the form \([L]^\mu\), where \(\mu\) is a value. Expressions may include neither memory locations nor the operator \([L]^\mu\). In our example language, we update the syntax of commands:

\[
C ::= \ldots \mid r := [L]^\mu; C \mid [L]^\mu := M; C
\]

Address calculation can be encoded using the conditional. We give the semantics simply by expanding this encoding. Applying this technique to Candidate 2.6, we arrive at the following:

\[
[r := [L]^\mu; C] \triangleq \{\ell (L = \ell) \triangleright (\bigcup_v (R^\mu [\ell] v) \Rightarrow [C] [[\ell]] / r)\}
\]

\[
[[L]^\mu := M; C] \triangleq \{\ell (L = \ell) \triangleright (\bigcup_v (M = v \mid W^\mu [\ell] v) \Rightarrow [C] [M/[\ell]])\}
\]

The same technique to be applied can be used to Definition 4.1—we elide the lengthy but obvious definition. For degenerate programs that include only constant references (every expression \([L]^\mu\) satisfies \(L = \ell\), for some \(\ell\), the resulting definition produces exactly the same executions as before.

The rewrites listed in §3-4 remain valid, with the following generalization: For address expressions \([M]\) and \([N]\), replace \(x = y\) by provable equality of \(M\) and \(N\), and \(x \neq y\) by provable inequality.

In Definition 4.1, we were able to ensure disjunction closure by performing targeted, local weakening via \(\text{weaken}_{\text{rax}}\) and \(\text{weaken}_{\text{wxM}}\). This is much more difficult to do with address calculation, since a single bit of syntax can refer to multiple locations. Consider that \([[r := 0]; [0] := !r]]\) includes both of the following pomsets ("!" is logical negation: "!M" evaluates to 1 if \(M\) is 0, and 0 otherwise):

\[
d: [r = 0 \mid W[0]0] \quad e: [r = 0 \mid W[0]1] \quad c: [r = 1 \mid W[1]0] \quad d: [r = 1 \mid W[0]0]
\]

Thus, the disjunction closure also includes both of the following:

\[
d: r = 0 \lor r = 1 \mid W[0]0 \quad e: r = 0 \lor r = 1 \mid W[0]1 \quad c: r = 1 \mid W[1]0 \quad d: r = 0 \lor r = 1 \mid W[0]0
\]

In this example, the \(d\) events that coalesce correspond to different statements in the syntax.
Because we do not enforce order between reads, there is some danger that address calculations could introduce anomalous behaviors that arise out of thin air (oota). Consider the following program, where initially $x = 0$, $y = 0$, $[0] = 0$, $[1] = 2$, and $[2] = 1$. It should only be possible to read 0, disallowing the attempted execution below:

$$r := y; s := [r]; x := s \quad \text{and} \quad r := x; s := [r]; y := s$$

(oota3)

Although no order is enforced between reads, the read-to-write order induced by the semantics is sufficient to prohibit this oota behavior. Note the intermediate state of $[s := [r]; x := s]$:

The precondition on $(Wx1)$ is required by causal strengthening (Def. 2.2).

6 UNDERSTANDING “OUT OF THIN AIR” USING TEMPORAL LOGIC

A significant challenge for a software memory model is to relax order enough to allow efficient implementation without admitting anomalous behaviors—called out of thin air (oota) in the literature [Batty et al. 2015; Boehm 2018; McKenney et al. 2016]. The most famous example is oota2 from §1. Here we inline initialization in order to fit the format of our proof rules:

$$y := 0; y := x \quad \text{and} \quad x := 0; r := y; x := r$$

(oota2)

Although Java does not allow oota behaviors of oota2, Lochbihler [2013] showed that it does allow oota behaviors of oota1, from §1. In [Jeffrey and Riely 2016], we described a logic that rules out oota2 but not oota1. In this section, we provide a more accurate test of oota behaviors by enhancing our previous logic with temporal features.

On first read, we suggest that readers skip to the examples and the discussion that follows, coming back to the details of the logic as necessary. Example 6.2 discusses the canonical oota example oota2; the analysis is trivial and well-known [Jeffrey and Riely 2016; Kang et al. 2017]. Example 6.3 is more interesting. There, we discuss a variant of Lochbihler’s example oota1, from the introduction.

The logic given here is not meant to be definitive; in §10, we discuss oota examples that require non-trivial extensions [Chakraborty and Vafeiadis 2019; Svendsen et al. 2018].

We adapt past linear temporal logic (PLTL) [Lichtenstein et al. 1985] to pomsets by dropping the previous instant operator and adopting strict versions of the temporal operators. The atoms of our logic are write and read events. Given a pomset $P$ and event $e$, define:

$$P, e \models Wxv \quad \text{if} \quad A(e) = Wxv \quad \text{and} \quad \text{true implies } \Phi(e)$$
$$P, e \models Rxv \quad \text{if} \quad A(e) = Rxv \quad \text{and} \quad \text{true implies } \Phi(e)$$
$$P, e \models q \land \delta \quad \text{if} \quad P, e \models q \quad \text{and} \quad P, e \models \delta$$
$$P, e \models \text{true}$$
$$P, e \models \neg q \quad \text{if} \quad P, e \not\models q$$
$$P, e \models \forall q \quad \text{if} \quad \forall d < e. P, d \models q$$
$$P, e \models \exists q \quad \text{if} \quad \exists d < e. P, d \models q$$

Define false, $\lor$, and $\Rightarrow$ as usual.

Let $P \models q$ if $P, e \models q$, for all $e \in E$.

Let $P \models q$ if $P \models q$, for all $P \in P$.

Let $q, P \models \delta$ if $\{P \mid P \models q\} \parallel P \models \delta$.

Let $q$ be downclosed when $\{P \mid P \models q\}$ is.
The past operators do not include the current instant, and so do not satisfy \(\Box q \Rightarrow \Diamond q\). The order-minimal elements always validate \(\Box q\) and invalidate \(\Diamond q\). However, we can prove the following:

\[
\begin{align*}
P \models (\Box q \Rightarrow q) & \Rightarrow q & \text{(Induction)} \\
P \models (q \Rightarrow \Box q) & \Rightarrow \neg q & \text{(Coinduction)} \\
P \models (q \Rightarrow \Diamond \delta) & \Rightarrow (\Diamond q \Rightarrow \Diamond \delta) & \text{(Weakening)}
\end{align*}
\]

We present two additional proof rules. The first provides a logical view of \(x\)-closure (Def. 2.7):

\[
\begin{align*}
g \text{ is independent of } x & \quad P \models (Rxv \Rightarrow \Diamond Wxv) \Rightarrow q \\
\forall x. P \models q
\end{align*}
\]

The second rule describes concurrent composition, in the style of Abadi and Lamport [1993]. To simplify the presentation, we consider the special case with a single invariant.

**Proposition 6.1.** Let \(q\) be downclosed. Let \(\mathcal{P}_1, \mathcal{P}_2\) be augmentation-closed. Then:

\[
g, \mathcal{P}_1 \models q \quad g, \mathcal{P}_2 \models q
\]

\[
\mathcal{P}_1 \parallel \mathcal{P}_2 \models q
\]

**Proof sketch.** We will show that all downsets in the downset closures of \(\mathcal{P}_1 \parallel \mathcal{P}_2\) satisfy the required property. Proof proceeds by induction on downsets of \(P \in \mathcal{P}_1 \parallel \mathcal{P}_2\). The case for empty downset follows from assumption that \(q\) is downset closed. For the inductive case, consider \(P \in \mathcal{P}_1 \parallel \mathcal{P}_2\) where \(P_i \in \mathcal{P}_i\). Since \(\mathcal{P}_1\) and \(\mathcal{P}_2\) are augmentation closed, we can assume that the restriction of \(P\) to the events of \(P_i\) coincides with \(P_i\), for \(i = 1, 2\). Consider a downset \(P'\) derived by removing a maximal element \(e\) from \(P\). Suppose \(e\) comes from \(P_1\) (the other case is symmetric). Since \(P_2\) is a downset of \(P'\) and \(P' \models q\) by induction hypothesis, we deduce that \(P_2 \models q\). Since \(P_1 \in \mathcal{P}_1\), by assumption \(g, \mathcal{P}_1 \models q\) we deduce that \(P \models q\).

**Example 6.2.** With all variables initialized to 0, we show that \textsc{oota2} satisfies \(\neg Wx1\).

We start with the invariant:

\[
[Wx1 \Rightarrow \Diamond Ry1] \land [Wy1 \Rightarrow \Diamond Rx1]
\]

This invariant holds for each thread; thus, it holds for the aggregate program by composition. Closing \(y\) yields \(Ry1 \Rightarrow \Diamond Wy1\). Weakening the right conjunct: \(\Diamond Wy1 \Rightarrow \Diamond Rx1\). Chaining these together: \(Ry1 \Rightarrow \Diamond Rx1\). Weakening: \(\Diamond Ry1 \Rightarrow \Diamond Rx1\). Chaining into the left conjunct: \(Wx1 \Rightarrow \Diamond Rx1\). Closing \(x\), weakening, then chaining: \(Wx1 \Rightarrow \Diamond Wx1\). By coinduction, \(\neg Wx1\).

The same reasoning can be applied to the control flow variant of \textsc{oota2} [Vafeiadis et al. 2015, CYC]: if (\(x\)\{\(y\): = 1\} \parallel if (\(y\)\{\(x\): = 1\}). The program is data-race-free. Thus, allowing an execution that writes 1 would violate sc-drf.

**Example 6.3.** The essential temporal property of \textsc{oota1} is: allocation at type \(\mathcal{C}\) is preceded by reading 0 for \(z\). Because our language lacks object creation, we cannot consider \textsc{oota1} directly. Instead we study \textsc{oota4}, which has the same temporal structure: writing 1 for \(x\) is preceded by reading 0 for \(z\). We show an attempted execution that violates this invariant:

\[
y:=0; \quad y:=x \quad x:=0; \quad a:=0; \quad \text{if}\{z\}\{r:=y; \; x:=r; \; a:=r\} \quad \text{else} \{x:=1\} \quad z:=0; \quad z:=1
\]

\[
\begin{align*}
& \text{Wy0} \quad \text{Ry1} \quad \text{Wy1} \quad \text{Wx0} \quad \text{Wa0} \quad \text{Rz1} \quad \text{Ry1} \quad \text{Wx1} \quad \text{Wa1} \quad \text{Wz0} \quad \text{Wz1}
\end{align*}
\]

We include location \(a\) to indicate the branch taken. The outcome is disallowed, due to the cycle. This outcome is also disallowed by our event structures model [Jeffrey and Riely 2019, §9], although the logic given in that paper is insufficient to establish this fact. The outcome is allowed by [Jagadeesan et al. 2010], [Kang et al. 2017], and [Chakraborty and Vafeiadis 2019].
To establish that this outcome is disallowed here, we prove \( \neg W_{a1} \), starting with invariant:
\[
[\Diamond Wy_1 \Rightarrow \Box R x_1] \land [W_{a1} \Rightarrow (\Diamond R y_1 \land \Box (W x_1 \Rightarrow \Diamond R y_1))]
\]
Closing \( y \) and chaining into the left conjunct: \( \Diamond R y_1 \Rightarrow \Diamond R x_1 \). Chaining into the right conjunct:
\[
W_{a1} \Rightarrow (\Diamond R x_1 \land \Box (W x_1 \Rightarrow \Diamond R x_1))
\]
Closing \( x \): \( W_{a1} \Rightarrow (\Diamond W x_1 \land \Box (W x_1 \Rightarrow \Diamond W x_1)) \). Applying coinduction to the right conjunct:
\[
W_{a1} \Rightarrow (\Diamond W x_1 \land \Box (\neg W x_1))
\]
Simplifying: \( W_{a1} \Rightarrow \text{false} \), as required.

Many examples are superficially similar, but in fact have fewer dependencies, such as \((\ast)\) from §1. **Boehm’s** [2018] **RFUB** example presents another potential form of **OOTa** behavior. Our analysis shows that there is no **OOTa** behavior in **RFUB**, only a false dependency:
\[
[r := y; x := r] \notin [r := y; if(r\neq 1)\{z := 1; r := 1\}; x := r] \quad \text{(RFUB)}
\]
The left command is half of **OOTa2**. The right command is dubbed **RFUB**, for *Register assignment From an Unexecuted Branch*. **Boehm** observes that in the context \( x := y \parallel [\ast] \), these programs have different behaviors. Yet the **OOTa** example on the left never writes \( 1 \). Why should the unexecuted branch change that? Because of the conditional, the write to \( x \) in **RFUB** is independent of the read from \( y \). It useful to considering the Hoare logic formulas satisfied by the two threads above: we have \{true\} **RFUB** \( \{x = 1\} \), but not \{true\} **OOTa** \( \{x = 1\} \). The change in the thread from **OOTa2** to **RFUB** is not a valid refinement under Hoare logic; as a result, it is expected that **RFUB** may have additional behaviors.

Understanding **OOTa** behavior is notoriously difficult, even for the greatest minds in the field! This example shows the wisdom of using existing tools, such as preconditions and Hoare logic, to model new problems, such as relaxed memory.

## 7 EFFICIENT IMPLEMENTATION ON ARM8

We show that our semantics compiles efficiently to **ARM8** [Deacon 2017; Pulte et al. 2018] using the translation strategy of Podkopaev et al. [2019], which was extended to SC access by Moiseenko et al. [2019, §5]: Relaxed access is implemented using 1dr/str, non-relaxed access using 1dar/stlr, acquire and other fences using dmb.1d/dmb.sy.

We consider the fragment of our language where concurrent composition occurs only at top level and there are no local declarations of the form (\( \textit{var} \ x; \ C \)). We show that any consistent **ARM8** execution graph for this sublanguage can be considered a top-level execution of our semantics. The key step is constructing the order for the derived pomset candidate. We would like to take \( \leq = (\textit{ob} \cup \textit{eco})^* \), where \textit{ob} is the **ARM8** acyclicity relation, and \textit{eco} is the **ARM8** extended coherence order. But this does not quite work.

The definition is complicated by **ARM8**’s *internal reads*, manifest in \( \textit{rfi} \), which relates reads to writes that are fulfilled by the same thread. **ARM8** drops \textit{ob}-order into an internal read. As discussed in §3.1, however, our semantics drops pomset order *out of* an internal read. To accommodate this, we drop these dependencies from the **ARM8** *dependency order before* (\textit{dob}) relation. The relation \textit{dob'} is defined from \textit{dob} by restricting the order into and out of a read that is in the codomain of the \( \textit{rfi} \) relation. More formally, let \( d \xrightarrow{\textit{dob'}} e \) when \( d \xrightarrow{\textit{dob}} e \) and \( d \notin \text{dom}(\textit{rfi}) \), \( e \notin \text{dom}(\textit{rfi}) \). Let \textit{ob'} be defined as for \textit{ob}, simply replacing \textit{dob} with \textit{dob'}.

For pomset order, we then take \( \leq = (\textit{ob'} \cup \textit{eco})^* \).

**Theorem 7.1.** For any consistent **ARM8** execution graph, the constructed candidate is a top-level memory model pomset.
The proof for compilation into tso is very similar. The necessary properties hold for tso, where ob is replaced by (the transitive closure of) the tso propagation relation [Alglave et al. 2014].

It is worth noting that efficient compilation is not possible for the earlier Flowing and Pop model [Flur et al. 2016], referenced in [Lahav and Vafeiadis 2016, Fig. 4], which allows the following:

\[
\begin{align*}
R_x1 & \xrightarrow{d} W_x1 & R_x1 & \xrightarrow{y} W_y1 & R_y1 & \xrightarrow{e} W_x1
\end{align*}
\]

This type of "big detour" [Alglave et al. 2014] is outlawed by arm8.3

8 LOCAL DATA RACE FREEDOM AND SEQUENTIAL CONSISTENCY

We adapt Dolan et al.’s [2018] notion of Local Data Race Freedom (LDRF) to our setting.

The result requires that locations are properly initialized. We assume a sufficient condition: that programs have the form "x₁ := v₁; \ldots; xₙ := vₙ; C" where every location mentioned in C is some xᵢ.

We make two further restrictions to simplify the exposition. To simplify the definition of happens-before, we ban fences and rmws. To simplify the proof, we assume there are no local declarations of the form (var x; C).

To state the theorem, we require several technical definitions. The reader unfamiliar with [Dolan et al. 2018] may prefer to skip to the examples in the proof sketch, referring back as needed.

**Data Race.** Data races are defined using program order (po), not pomset order (≤). In SB, for example, (Rx0) has an x-race with (Wx1), but not (Wx0), which is po-before it.

It is obvious how to enhance the semantics of prefixing and most other operators to define po. When combining pomsets using the conditional, the obvious definition may result in cycles, since po-ordered reads may coalesce. In this case we include a separate pomset for each way of breaking these cycles.

Because we ignore the features of §5, we can adopt the simplest definition of synchronizes-with (sw): Let \( d \xrightarrow{sw} e \) exactly when d fulfills e, d is a release, e is an acquire, and \( \neg(d \xrightarrow{po} e) \).

Let \( \text{hb} = (\text{po} \cup \text{sw})^+ \) be the happens-before relation. In PUB1, for example, \((Wx1)\) happens-before \((Rx0)\), but this fails if either ra access is relaxed.

Let \( L \subseteq X \) be a set of locations. We say that \( d \) has an L-race with \( e \) (notation \( d \xrightarrow{\text{hb}} e \)) when they conflict (Def. 2.7) at some location in \( L \), but are unordered by \( \text{hb} \): neither \( d \xrightarrow{\text{hb}} e \) nor \( e \xrightarrow{\text{hb}} d \).

**Generators.** We say that \( P' \) generates \( P \) if either \( P \) augments \( P' \) or \( P \) implies \( P' \). For example, the unordered pomset \((Rx1)\) \((Wy1)\) generates the ordered pomset \((Rx1) \rightarrow (r = 1 \mid Wy1)\).

We say that \( P \) is a generation-minimal in \( \mathcal{P} \) if \( P \in \mathcal{P} \) and there is no \( P \neq P' \in \mathcal{P} \) that generates \( P \). Let \( \text{gen}[C] = \{ P \in [C] \mid P \text{ is top-level and generation-minimal in } [C] \} \).

**Extensions.** We say that \( P' \) C-extends \( P \) if \( P \neq P' \in \text{gen}[C] \) and \( P \) is a downset of \( P' \).

**Similarity.** We say that \( P' \) is e-similar to \( P \) if they differ at most in (1) pomset order adjacent to \( e \) and (2) the value associated with event \( e \), if it is a read. Formally: \( E' = E, \Phi' = \Phi, \leq'[e|E\setminus{e}] = \leq[|E\setminus{e}] \), if \( e \) is not a read then \( \mathcal{A}' = \mathcal{A} \), and if \( e \) is a read then \( \mathcal{A}'|_{E\setminus{e}} = \mathcal{A}|_{E\setminus{e}} \) and \( \mathcal{A}'(e) = \mathcal{A}(e)[\nu'/\nu] \), for some \( \nu', \nu \).

**Stability.** We say that \( P \) is L-stable in \( C \) if (1) \( P \in \text{gen}[C] \), (2) \( P \) is po-convex (nothing missing in program order), and (3) there is no C-extension of \( P \) with a crossing L-race: that is, there is no \( d \in E, \text{ no } P' \text{-C-extending } P \), and no \( e \in E' \setminus E \) such that \( d \xrightarrow{\text{hb}} e \). The empty pomset is L-stable.

3There is either a cycle \( R_x1 \xrightarrow{\text{poloc}} d \xrightarrow{\text{co}} e \xrightarrow{\text{dr}} R_x1 \) or \( d \xrightarrow{\text{dr}} R_x1 \xrightarrow{\text{data}} W_y1 \xrightarrow{\text{dr}} R_y1 \xrightarrow{\text{data}} e \xrightarrow{\text{co}} d \).
Sequentiality. Let $\ll_L = \ll_L \cup \text{po}$, where $\ll_L$ is the restriction of $<$ to events that access locations in $L$. We say that $P'$ is $L$-sequential after $P$ if $P'$ is $\text{po}$-convex and $\ll_L$ is acyclic in $E' \setminus E$.

**Theorem 8.1.** Let $P$ be $L$-stable in $C$. Let $P'$ be a $C$-extension of $P$ that is $L$-sequential after $P$. Let $P''$ be a $C$-extension of $P'$ that is $\text{po}$-convex, such that no subset of $E''$ satisfies these criteria. Then either (1) $P''$ is $L$-sequential after $P$ or (2) there is some $C$-extension $P'''$ of $P'$ and some $e \in (E'' \setminus E')$ such that (a) $P'''$ is $e$-similar to $P''$, (b) $P'''$ is $L$-sequential after $P$, and (c) $d \not\stackrel{\text{wr}}{\sim} e$, for some $d \in (E'' \setminus E)$.

The theorem provides an inductive characterization of Sequential Consistency for Local Data-Race Freedom (SC-LDRF): Any extension of a $L$-stable pomset is either $L$-sequential, or is $e$-similar to a $L$-sequential extension that includes a race involving $e$.

**Proof Sketch.** In order to develop a technique to find $P'''$ from $P''$, we analyze pomset order in generation-minimal top-level pomsets. First, we note that $\ll_L$ (the transitive reduction $\ll_L$) can be decomposed into three disjoint relations. Let $\text{ppo} = (\ll_L \cap \text{po})$ denote preserved program order, as required by prefixing (Def. 2.6). The other two relations are cross-thread subsets of $(\ll_L \setminus \text{po})$, as required by fulfillment (Def. 2.7): wr orders writes before reads, satisfying fulfillment requirement $\text{F}3$; $\text{xw}$ orders read and write accesses before writes, satisfying requirement $\text{F}4$. (Within a thread, $\text{F}3$ and $\text{F}4$ follow from prefixing requirement $\text{p5b}$, which is included in $\text{ppo}$.)

Using this decomposition, we can show the following.

**Lemma 8.2.** Suppose $P'' \in \text{gen}[C]$ has a read $e$ that is maximal in $(\text{ppo} \cup \text{wr})$ and such that every $\text{po}$-following read is also $\ll_L$-following ($e \ll_L d$ implies $e \ll d$, for every read $d$). Further, suppose there is an $e$-similar $P'''$ that satisfies the requirements of fulfillment. Then $P''' \in \text{gen}[C]$.

The proof of the lemma follows an inductive construction of gen[C], starting from a large set with little order, and pruning the set as order is added: We begin with all pomsets generated by the semantics without imposing the requirements of fulfillment (including only $\text{ppo}$). We then prune reads which cannot be fulfilled, starting with those that are minimally ordered. This proof is simplified by precluding local declarations.

We can prove a similar result for $(\text{po} \cup \text{wr})$-maximal read and write accesses.

Turning to the proof of the theorem, if $P''$ is $L$-sequential after $P$, then the result follows from (1). Otherwise, there must be a $\ll_L$ cycle in $P''$ involving all of the actions in $(E'' \setminus E')$: If there were no such cycle, then $P''$ would be $L$-sequential; if there were elements outside the cycle, then there would be a subset of $E''$ that satisfies these criteria.

If there is a $(\text{po} \cup \text{wr})$-maximal access, we select one of these as $e$. If $e$ is a write, we reverse the outgoing order in $\text{xw}$; the ability to reverse this order witnesses the race. If $e$ is a read, we switch its fulfilling write to a “newer” one, updating $\text{xw}$; the ability to switch witnesses the race. For example, for $P''$ on the left below, we choose the $P'''$ on the right; $e$ is the read of $x$, which races with $(Wx1)$.

\[
x := 0; y := 0; (x := 1; y := 1) \quad \text{if} \{ y \{ r := x \}
\]

It is important that $e$ be $(\text{po} \cup \text{wr})$-maximal, not just $(\text{ppo} \cup \text{wr})$-maximal. The latter criterion would allow us to choose $e$ to be the read of $y$, but then there would be no $e$-similar pomset: if an execution reads 0 for $y$ then there is no read of $x$, due to the conditional.
Pomsets with Preconditions

If there is no \((po \cup wr)\)-maximal access, then all cross-thread order must be from \(wr\). In this case, we select a \((ppo \cup wr)\)-maximal read, switching its fulfilling write to an "older" one. As an example, consider the following; once again, \(e\) is the read of \(x\), which races with \((Wx1)\).

\[
x := 0; y := 0; (r := x; y := 1) \parallel s := y; x := s
\]

This example requires \((Wx0)\). Proper initialization ensures the existence of such "older" writes. □

The premises of the theorem allow us to avoid the complications caused by "mixed races" in [Dongol et al. 2019]. In the left pomset below, \(P''\) is not an extension of \(P'\), since \(P'\) is not a downset of \(P''\). When considering this pomset, we must perform the decomposition on the right.

\[
(x := 1; x'ra := 1) \parallel (r := x'ra)
\]

This affects the inductive order in which we move across pomsets, but does not affect the set of pomsets that are considered. This simplification is enabled by denotational reasoning.

In our language, past races are always resolved at a stable point, as in \(co3\). As another example, consider the following, which is disallowed here, but allowed by Java [Dolan et al. 2018, Ex. 2]. We include an SC fence here to mimic the behavior of volatiles in the JMM.

\[
(x := 1; y'ra := 1) \parallel (x := 2; F_{sc}; if(y'ra)\{r := x; s := x\})
\]

The highlighted events are \(L\)-stable. The order from \((Rx1)\) to \((Wx2)\) is required by fulfillment, causing the cycle. If the fence is removed, there would be no order from \((Wx2)\) to \((R'ra y1)\), the highlighted events would no longer be \(L\)-stable, and the execution would be allowed. This more relaxed notion of "past" is not expressible using Dolan et al.’s synchronization primitives.

The notion of "future" is also richer here. Consider [Dolan et al. 2018, Ex. 3]:

\[
(r := 1; [r] := 42; s := [r]; x'ra := r) \parallel (r := x; [r] := 7)
\]

There is no interesting stable point here. The execution is disallowed because of a read from the causal future. If we changed \(x'ra\) to \(x'rlx\), then there would be no order from \((R[1]7)\) to \((W'rlx x1)\), and the execution would be allowed. The distinction between "causal future" and "temporal future" is not expressible in Dolan et al.’s operational semantics.

Our definition of \(L\)-sequentiality does not quite correspond to SC executions, since actions may be elided by read or write elimination (§4). However, for any properly initialized \(L\)-sequential pomset that uses elimination, there is larger \(L\)-sequential pomset that does not use elimination.
This can be shown inductively: writes that are introduced this way can be ignored by existing reads; reads that are introduced this way can be fulfilled by some preceding write, using its value.

9 OTHER RELATED WORK

We survey related work not discussed previously.

A memory consistency model for a shared-memory multiprocessor defines the values that a read may return. For a survey of hardware models, see [Alglave 2010]. For software models, see [Batty 2015; Lochbihler 2013]. For an attempt to bridge the two, see [Podkopaev et al. 2019]. Pulte et al. [2019] present an operational model of ARM8 in the style of [Kang et al. 2017].

In our previous work [Disselkoen et al. 2019], we introduced the notion of pomsets with preconditions. In 2019, we studied micro-architecture, where failed speculative execution is visible via cache effects. Here we presented an architectural model, which allows us to impose consistency, ignoring failed speculative execution, and causal strengthening. In 2019, we used 3-valued pomsets, as opposed to the simple pomsets used here; see §10 for further discussion. The previous paper was not focused on memory models, and thus did not prove the soundness of compiler optimizations, the absence of thin air reads, efficient implementability, or sc-drf.

Our model shares important structural elements with that of Paviotti et al. [2020], who provide a fix for the thin-air problem in C11. Like us, they use true concurrency semantics to identify (in)dependence in an execution and thus calculate the preserved program order explicitly. Our definition of parallel composition allows events to coalesce, taking preconditions via disjunction—this is mirrored by Paviotti et al.’s definition of coproduct. We only compose downclosed pomsets—this is mirrored by their condition on $\leq_X$ during coproduct (discussed in their §6.3). Nonetheless, the papers have different goals, leading to different outcomes. For example, their model compiles efficiently to non-mca architectures; our model clearly does not! Conversely, our model provides an intrinsic characterization of optimizations, such as redundant read elimination, which only hold in their model up to observational refinement.

True concurrency techniques have been applied to relaxed memory by Cenciarelli et al. [2007], Castellan [2016], Pichon-Pharabod and Sewell [2016], and Chakraborty and Vafeiadis [2017]. See [Jeffrey and Riely 2019, §8] for a discussion. A partial order approach to weak memory was sketched by Brookes [2016] and fleshed out for TSO by Kavanagh and Brookes [2019]. Their action labels include buffers, encoding the operational behavior of TSO inside the pomsets themselves.

There is a rich literature on the use of transformations over SC executions to model relaxed memory: Saraswat et al. [2007] aimed to describe a jmm-like model this way. sc-drf holds, but Sevčík [2011] discovered that it permits oota behavior. Demange et al. [2013] developed BMM, which permits reordering of a relaxed write with a following relaxed read. BMM is designed as a restriction of the jmm that compiles efficiently to TSO. It requires fencing on other architectures. Lahav and Vafeiadis [2016] characterized TSO as being derived by considering Write-Read (WR) reordering and Read-After-Write (RAW) elimination. They also showed that the release acquires of C11 are less expressive than considering WR and RAW together with thread-inlining. Our paper is inspired by their implicit challenge: “Some memory models can be defined via transformations. But there is more to weak memory than transformations.”

10 LIMITATIONS

Our work has several limitations, each of which provides an opportunity for future research.

We have not modeled loops or functions. Loops and recursive functions introduce complexities—such as liveness and continuity—that are orthogonal to the main topic of the paper.

We have not modeled general sequencing of the form $(C; C')$. The definition of prefixing (§2.6) is relatively simple since we only prepend one action at a time.
We have not modeled mixed-size access [Flur et al. 2017; Watt et al. 2020]. ARM8 captures multibyte access using multiple events related by same instruction (si) [Alglave 2019]. To capture the use of si when defining locally ordered before (lob), it is likely sufficient to modify p5B. To capture the use of si when defining observation (ob), it is likely sufficient to modify f3 and f4.

We have not attempted validate all program transformations that involve synchronization, fences or rmws [Morisset 2017; Vafeiadis et al. 2015]. Nonetheless, our semantics validates roach motel (roach1, roach2), redundant load (rl), fence removal (rf), and store forwarding (sf). We expect that dead store elimination (ds) generalizes to non-relaxed access by generalizing cover, in Definition 4.1. Some transformations are not sound in the model, but we expect them to be provable as metaproperties. For example, access-mode strengthening (such as replacing rlx by ra) is valid up to an equivalence that ignores access modes on actions. Other transformations worth studying include commuting adjacent synchronizations and implementing non-relaxed access using relaxed access and fences. Lock elision and access-mode weakening are also interesting, although these are only sound in certain contexts. We expect all of these transformations to be valid, given an appropriate notion of validity.

The logic we presented in §6 is only strong enough to prove a few examples. Svendsen et al. [2018] presented a different a logic, capable of showing that the following program cannot write 2:

\[
(y := x + 1 \parallel x := y)
\]

The attempted execution is not allowed by our semantics, since there is no write to fulfill (Ry1). As another example, consider the following, from Chakraborty and Vafeiadis [2019, Fig. 3]:

\[
x := 2; \text{if}(x \neq 2)\{y := 1\} \parallel x := 1; \text{if}(y)\{x := 3\}
\]

The attempted execution is not allowed by our semantics, due to the evident cycle. Intuitively, it is not possible for the left thread to read 3 for x when the right thread reads 2. Proving this may require a logic with modalities to deal with intervening writes and coherence. Surprisingly, this outcome is allowed by the promising semantics [Kang et al. 2017]. Chakraborty and Vafeiadis developed weakestmo to address this example; however, weakestmo does not address oota4.

Our model realizes multi-copy atomicity (mca). Thus it will not compile efficiently to non-mca architectures, such as power and arm7. To do so, one cannot include the order required by f4 in pomset order. In [Disselkoen et al. 2019], we modeled programs using 3-valued pomsets, using the weak relation (\(\not\approx\)) for f4 and p5B. This does not provide a suitable model for non-mca behavior, however, since it disallows mca4.

In the discussion of mca2, we noted that our model does not enforce order between reads due to address and control dependencies. This has implications for Java’s final field semantics. Consider:

\[
(r := 1; \{r\} := \emptyset; \{r\} := 1; x^{ra} := r) \parallel (r := x^{ra}; s := [r])
\]

If we changed x^{ra} to x^{rlx}, then there would be no order from (Rx1) to (R[1]0), and the execution would be allowed. In order to allow this relaxation in certain cases without invalidating the publication of the “field initializer” (W[1]1), it may be desirable to distinguish address dependencies from other dependencies—doing so would likely require two separate preconditions for each event.

\[\text{4Following [Lamport 1986], 3-valued pomset require: (1) if } d \leq e \text{ then } d \not\approx e, (2) if } d \leq e \text{ and } e \not\approx d \text{ then } d = e, \text{ and (3) if } e \not\approx d \text{ then } e \not\approx d. \text{ mca2 is disallowed by (2). Top-level 3-valued pomsets also require that } \not\approx \text{ is a partial order per-location; a sufficient condition is (4) if } d \not\approx e \text{ and } e \not\approx d \text{ then } d \not\approx d \text{ and } e \not\approx d. \text{ Although mca1 is allowed, its two-thread variant is not, due to the combination of semi-transitivity (3) and partial coherence (4).}\]


